Amendments to the Drawings:

Figures 1 and 3 have been corrected to add descriptive labels for elements 12 and 14 of

Figure 1 and elements 22 and 24 of Figure 3. Two replacement sheets are attached for

showing these corrections. No new matter is added, and acceptance of the drawings is

5   respectfully requested.

Attachment: Replacement Sheets   2 pages

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REMARKS/ARGUMENTS

1. Objections to claims 1 and 15:

   Claims 1 and 15 are objected to due to informalities. In claim 1, "media control circuit" is suggested to change to --medium access control circuit--. In claim 15, "when" is suggested to change to --wherein--. Appropriate correction is required.

Response:

   Claims 1 and 15 have been amended to correct these informalities. Acceptance of the amended claims is respectfully requested.

2. Rejection of claim 14 under 35 U.S.C. 112, second paragraph:

   Claim 14 is rejected under 35 U.S.C. 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

   The recitation of "the error information" recited in claim 14 lacks antecedent basis.

Response:

   Claim 13 has been amended to change "other information" to become --other error information--. No new matter has been added, and claim 14 now contains no problem with antecedent basis. Reconsideration of claim 14 is respectfully requested.

3. Rejection of claims 1-20 under 35 U.S.C. 103(a):

   Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art of the instant application in view of Butler et al. (US 6,741,612, hereafter referred to as "Butler").

Response:

Claim 1 has been amended to overcome this rejection, and the applicant would like to point out the patentable limitations contained in independent claims 1 and 12.

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Claim 1 recites that the receiving-enabling interface (CRS_DV) detects a low-voltage for indicating an error-detection mode and an idle mode, and detects a high voltage for indicating a transmission-enabling mode. Furthermore, a data receiving interface (RXD) is used for transmitting the data from the physical circuit (PHY circuit) to the medium access control circuit (MAC circuit). By detecting the level of the voltage received through the receiving-enabling interface (CRS_DV), the MAC circuit can determine whether to receive the data transmitted from the data receiving interface (RXD) or to reject the data. Because of this, the MAC circuit does not need to know the current state of communication, and can simply judge the level of the voltage received through the receiving-enabling interface (CRS_DV) for determining whether to reject or receive data. A low voltage value received through the receiving-enabling interface (CRS_DV) represents either error-detection mode or idle mode, and the low voltage can be received at any time from the perspective of the MAC circuit regardless of state. In either case, the MAC circuit will reject the data.

Furthermore, Butler teaches combining the carrier sense (CRS) and the data valid (DV) signals on a single pin if the state is known. The present invention already makes use of this knowledge as evidenced by the signal "CRS_DV" received by the receiving-enabling interface. Thus, Butler repeats what is already well known in the art of RMII systems when stating that the carrier sense (CRS) and the data valid (DV) signals can be combined on a single pin if the state is known.

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As stated above, since the MAC circuit does not need information as to the state of communication, it is able to determine whether to accept or reject data based only on the level of the level of the voltage received through the receiving-enabling interface (CRS_DV). Therefore, the applicant submits that one skilled in the art would not find it obvious to combine the teachings of the admitted prior art and Butler for creating the claimed invention according to claim 1.

Independent claim 12 recites the limitations of:

"receiving the data transmitted from the physical circuit (PHY circuit) via the data receiving interface when the receiving-enabling interface detects a high voltage by using the medium access control circuit (MAC circuit); and

rejecting the data transmitted from the physical circuit (PHY circuit) via the data receiving interface when the receiving-enabling interface detects a low voltage by using the medium access control circuit (MAC circuit).
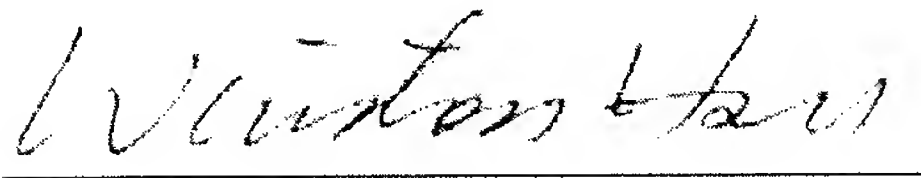
Therefore, claim 12 should be allowable for the same reasons as the currently amended claim 1. In addition, claims 4-11 and 13-20 are dependent on claims 1 and 12, and should be allowed if their respective base claims are allowed. Reconsideration of claims 1 and 4-20 is therefore respectfully requested.

In view of the claim amendments and the above arguments in favor of patentability, the applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

5   Sincerely yours,

Date: _____06.04.2007_____

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15   is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)